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Optimization of a CNTFET Based SRAM Cell Parameters

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Abstract

This research proposes an optimized set of parameters for a design of the 6-T (Six Transistor CMOS SRAM) SRAM cell using CNTFET technology. The CNTFET utilized a planar gate structure with multiple cylindrical conducting channels and high k (high dielectric constant) gate dielectric material on a substrate with a different dielectric. In addition, the Stanford CNTFET model has studied, which is organized hierarchically in three main levels to simulate a MOSFET-like CNFET device. The performance of the CNTFET-based (Carbon Nano Tube Field-Effect Transistor) SRAM (Static Random Access Memory) cell has evaluated using three main criteria: Static Noise Margin (SNM), Critical Write Time, and Standby Power. The optimization is conducted for two different voltage levels: 0.9V and 0.7V. The SNM is calculated using HSPICE simulation and the obtained data has utilized to optimize the CNTFET SRAM cell by varying chirality and channel length. Furthermore, a comparison of the three matrices for CNTFET, CMOS, and FinFET processes is conducted. The simulation results confirm that the CNTFET SRAM design is a significant improvement in Read SNM with superior writability and lower power consumption compared to CMOS and FinFET processes. Additionally, the simulation of SNM for a wide temperature range demonstrates that the CNTFET SRAM has a relatively stable response to temperature variations.

I. INTRODUCTION

The past two decades have seen a considerable advancement in memory technology for high-density data storage applications, including the Internet of Things, cloud computing, data science, data mining, artificial intelligence, machine learning, industrial robots, and cyber security [1]–[6]. SRAM (static RAM) is a type of random access memory (RAM) that retains data bits in its memory as long as power is being supplied. Three performances have been considered as the main criteria for the optimization of SRAM cell: Static noise margin, Critical write time and Stand by power. Using one of the methods, SNM data is obtained for CNTFET SRAM cell. A superior performance of CNTFET is designed by optimizing it's different parameters as chirality, channel etc. The delay between read and write speeds may be used to assess the performance of any type of memory chip [7]- [8]. For both read and write operations, various memory types have varying access rates. Semiconductor memory may generally be divided into two categories. The first is referred to as volatile (RAM) memory, and the second as nonvolatile (ROM). DRAM and SRAM are the two fundamental kinds of RAM, whereas ROM comes in a variety of forms, including Bi-CMOS ROM, Masked ROM, PROM, EPROM (used in FAMOS devices), EEPROM (used in FLOTOX devices), and NAND and NOR Flash [9]–[15]. In depth research is being done on the spin-based magneto resistive RAM (MRAM) [16]-[17]. Gallium arsenide FeRAM (GaAsFeRAM), for instance, is a form of nonvolatile memory that is employed in a number of applications. Ferroelectric characteristics are utilized in these memory devices to keep the information after the power is turned off. Several research teams have developed nonvolatile SRAM. A type of memory called nonvolatile SRAM can continue to store data or digital bits even when the power source is turned off. A single 6T-SRAM cell and twin floating gate (twin floating gate nano transistor is a kind of floating gate MOSFET) transistors make up nonvolatile SRAM [18],-[19].

According to reports, almost 90%–95% of integrated circuits (ICs) generate 51% of the delay due to incorrect modeling of the interconnect and 49% of the delay due to gate or device delay [20]-[21]. RC (the delay in signal speed through the circuit wiring delay), or interconnect delay, is more important in memory circuits than gate or device delay. The standard Cu connection exhibits a significant degree of interconnect delay as a result of its greater interconnect resistance at nanoscale dimensions. According to recent studies, multilayered graphene nanoribbon (MLGNR) interconnects are among the most promising materials for interconnect modeling for next-generation ICs design because of their lower resistivity compared to Cu interconnects, high current density (roughly 5- 20 108 A/cm2), and long electron mean free path (300 nm-1000 nm) [21],-[22]. Electron transport characteristics are practically ballistic compared to other conventional nano-interconnect materials (Cu, Al, Ni, and so on) [20],-[21], which have an electron mean free path (300 nm–1000 nm) [23]–[27]. It is a stack of top contact (TCGNR) and side-contact (SC-GNR) contacts with different contact resistances that make up single layer GNR (SLGNR) structures [24]. Due to its decreased resistivity, MLGNR exhibits a minor IR-drop in the power distribution network. In this work, a 16-nm PTM-HPC CMOS model has been used to create a 6TSRAM cell. The SRAM cell is designed with a temperature-dependent MLGNR connection, and read speed delay vs Cu interconnects is utilized to compare the results. For the upcoming generation of high-performance memory circuit designs, this is a revolutionary strategy. This study examines the effects of NBTI (Negative Bias Temperature Instability) on the read and write operation delays and power consumption of the 6T SRAM circuit. Several types of failure mechanisms have used to investigate the performances. Including the oxide trap and interface, as well as varied operating temperatures and stress time conditions. Additionally, read and write operations have evaluated in terms of circuit delay and power consumption.

II. LITERATURE REVIEW

The advancement of semiconductor technology has led to the development of various types of Static Random Access Memory (SRAM) cells. Researchers have extensively explored and compared different SRAM cell designs to improve performance and efficiency. This literature review has discussed many research papers that analyze the characteristics of 6T, 7T, 8T, and 9T SRAM cells. These studies provide insights into the read delay, write delay, power consumption, noise margin, and other vital metrics associated with these SRAM cells. The papers contribute to understanding SRAM cell behavior and provide valuable information for designing efficient memory systems. Deepak et. al conducted a comparative study in their research paper, where they evaluated the performance of 6T SRAM cells against 7T, 8T, and 9T SRAM cells [28]. The analysis encompassed read delay, write delay, read power, write power, Read Static Noise Margin (RSNM), and Write Static Noise Margin (WSNM). To conduct their experiments, the researchers utilized the Cadence Spectre test system. The findings of their study shed light on the trade-offs between different SRAM cell designs, allowing designers to make informed decisions regarding selecting an appropriate cell configuration based on specific requirements. In another work has presented by Rizvi et. al a subjective method was employed to evaluate the behavior of a 6T SRAM cell under the influence of power supply noise and inverter latch noise [29]. This study has been performed using a 180nm CMOS process. The researchers focused on examining the Write Margin, Write Time and Static Noise Margin while inducing noise. The subjective approach adopted in this research offers insights into the robustness and reliability of the 6T SRAM cell under noisy conditions, which is crucial for designing memory systems that can withstand real world operating environments. Premalatha et. al addressed the issue of power distribution in SRAM cells during writing and reading activities in their research. They proposed a dual limit voltage solution for 6T, 7T, 8T, and 9T SRAM cells [30]. The researchers have analyzed these cells' delay and power propagation characteristics using the Cadence Virtuoso tools and Spectre as the test system. Their study was conducted on the 90nm Generic Process Design Kit. The findings of this research contribute to the development of power efficient SRAM designs by managing power distribution effectively, thereby enabling the design of energy efficient memory systems.

In conclusion, the three research papers reviewed in this literature review provide valuable insights into the behavior and performance of different SRAM cell configurations. The comparative study by Deepak et. al offers a comprehensive analysis of the trade-offs between 6T, 7T, 8T, and 9T SRAM cells regarding read delay, write delay, power consumption, and noise margins [28]. The work presented by Rizvi et. al explores the impact of noise on the 6T SRAM cell, providing insights into its robustness under noisy conditions [29]. Additionally, the research conducted by Premalatha et. al addresses power distribution issues in SRAM cells. It proposes a dual-limit voltage approach to improve power efficiency. Collectively, these studies contribute to the understanding and optimization of SRAM cell designs for efficient memory system [30].

III. CNTFET SRAM Simulation Methodology

A. Design and use of the 6T SRAM under NBTI deterioration:

The design for the 6T SRAM circuit utilized in this work is shown in **“figure 1”.** The DSCH simulation (DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started) program has utilized in the creation of the 6T SRAM. In reality, the RAM cell area determine the device sizes. The transistor size for both read and write operations is, as a general rule, 3/2. The pull-up PMOS transistor size is twice or three times wider than the pulldown NMOS transistor because NMOS has a mobility that is three times that of PMOS. The 16 nm bulk tri-gate FinFET Predictive Technology Model has employed in this work [31]. The Synopsis simulator has been utilized to do additional reliability study using the circuit’s netlist. The transistor P1 will experience NBTI degradation because its gate to source voltage is negative (-VDD volts) and the drain to source voltage is zero volts, which is necessary for NBTI degradation to take place. This is assuming that the internal node is storing a logic “0” and Q is storing a logic “1”. The performance of 6T SRAM cells would suffer due to the threshold voltage, which will also have an impact on other crucial SRAM performance factors including SNM, read latency, and write delay [32].

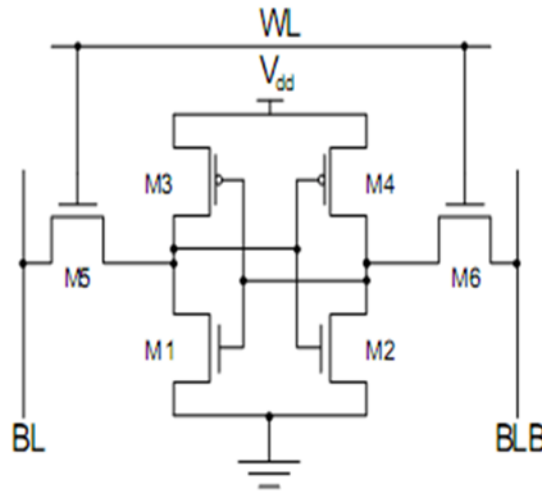

Figure 1 :The schematic of 6T SRAM

B . SRAM Cell Architecture :

As illustrated in “**figure 2”,** the fundamental structure of an SRAM consists of one or more rectangular arrays of memory cells with supporting circuitry to decode addresses and carry out the necessary read and write operations [33]. SRAM memories, also referred to as word-lines and bit-lines, are organized in rows and columns, and each of them has a specific position determined by the point where the rows and columns cross. There is a specific data input/output (I/O) pin associated with each address. The overall amount of memory, the speed at which memory must work, the layout, and the quantity of data I/Os on the chip all influence how many arrays are present in a memory chip. It may be set up to be word-oriented or bit-oriented. “**figure 2”** displays a diagram of the SRAM selling architecture. A row decoder gated by appropriate timing block signal decodes X row address bits and selects on of the word lines WL 0–WL N-1. The SRAM core consists of a number of arrays of NxM, where N is the number of rows and M is the number of bits. If an SRAM core is organized as a number of arrays in a page manner, an additional Z-decoder is needed to select the accessed page, “**figure 3**” shows an example of an SRAM with four pages of NxM arrays with the corresponding I/O blocks [34].

C. Model of Six-Transistor (6T) SRAM Cell

The static latch, which consists of two cross-coupled inverters, is included into the six transistor SRAM cell. Therefore, as long as the cell has a sufficient power supply, the stored information may be retained without needing to be refreshed on a regular basis. It has six transistors, just as one type of SR latch implementation. Cross-coupled CMOS inverters are made up of four transistors (Q1–Q4), and read and write access to the cell is provided by the two NMOS transistors Q5 and Q6 [35]. The access transistors join the two internal nodes of the cell to the true (BL) and complementary (BLB) bit lines upon word line activation.

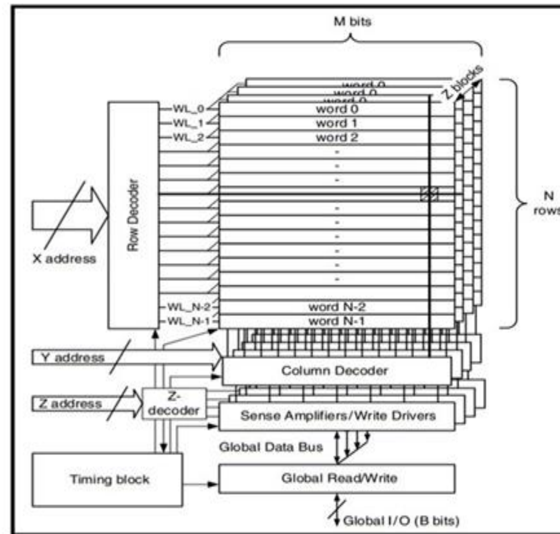

Figure 2 : SRAM block diagram

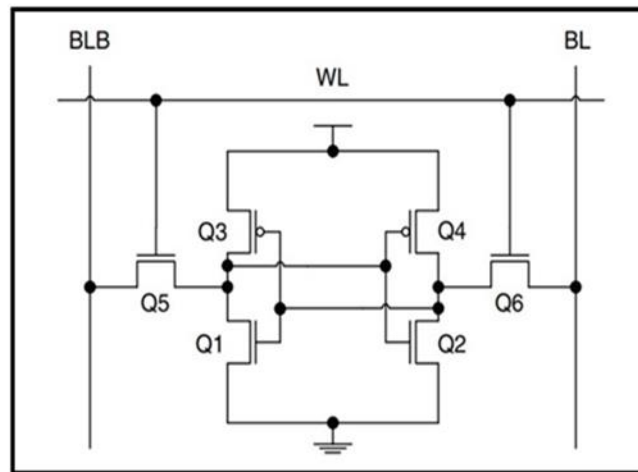

Figure 3: Six-transistor(6T) CMOS SRAM CELL

D. Read Operation

Before a read operation is initiated, bit lines are pre-charged to VDD. The read procedure is initiated by activating the word line (WL) and connecting the precharged bit lines (BL and BLB) to the

internal nodes of the cell. In the read access shown in **“figure 4’**, the bit line voltage VBL remains constant and remains at the precharged level. To discharge the complimentary bit line voltage VBLB, transistors M1 and M5 are connected in series. As a result, transistors M1 and M5 build a voltage divider whose output is now connected to the input of inverters M2-M4 and is not zero volts. The sizing of M1 and M5 should prevent destructive reads from occurring if inverter M2-M4 switches. In other words, 0+V should be lower than the inverter M2–M4 switching threshold plus a safety buffer or noise margin [36].

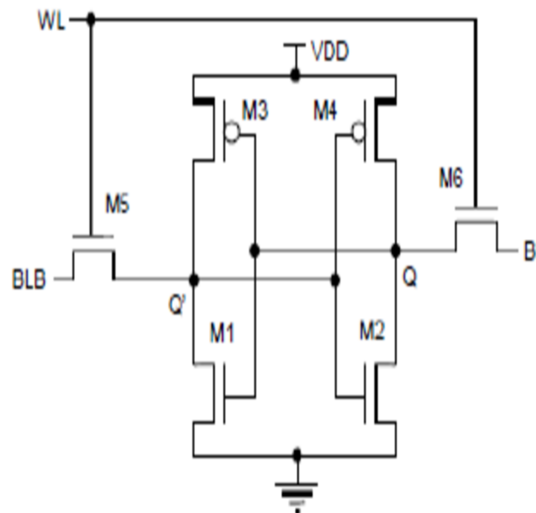

Figure 4 : SRAM read operation

E. SRAM Cell Static Noise Margin

Noise margin is a measurement of design margins used to guarantee that circuits will operate correctly under specific circumstances. Noise Margin (NM) is often defined as the greatest erroneous signal that a device may take in a system while continuing to function correctly [37]. It is presumed that the noise is “static” or dc and has been there long enough for the circuit to respond [38]. This approach has a significant benefit in that it may be automated using a DC circuit simulator, greatly increasing its practical applicability. “**figure 5”** [12] in an x-y coordinate system displays the overlaid normal inverter transfer curve of a read- accessed 6T SRAM cell and its counterpart that is mirrored with regard to the x=y line. With regard to the x-y coordinate system, the u-v coordinate system is rotated 45 degrees counterclockwise around the same origin [13]. This setup is practical. Since the sides may be determined by knowing the diagonals of the largest embedded squares. The sought-after diagonals are parallel to the v axis. **“Figure 5”** estimates ”maximum squares” in a 45° rotated coordinate system is represented by the dotted curve in the u-v coordinate system. An SRAM cell’s two inverters’ voltage transfer characteristics (VTCs) are perfectly symmetrical [39]. The x-y coordinate system’s subtraction of the normal and mirrored inverter transfer curves. The extremities of this curve correspond to the diagonals of the maximum embedded squares since squares are at their largest when the lengths of their diagonals D1 and D2 are at their maximum. D1 = D2 is a common result of the process spread. Assume that D1 exceeds D2. D1/2 then produces the flip-flop’s SNM. The following mathematical formulation can be used to express the aforementioned algorithm. Assume that the functions

y = F1(x) and y = F2(x), the latter of which is the mirrored form of y = F2(x). The x-y coordinate system must be changed as described below in order to determine F1 in terms of u and v [40]:

$$x = \frac{1}{\sqrt{2}}U + \frac{1}{\sqrt{2}}v \quad (1)$$

$$y = -\frac{1}{\sqrt{2}}U + \frac{1}{\sqrt{2}} \quad (2)$$

Substitution of Equations (1) and (2) in y = F1(x) gives: $v = U + \sqrt{2}F_1(\frac{1}{\sqrt{2}}U + \frac{1}{\sqrt{2}}v)$ (3)

F2 is first mirrored in the x-y system with respect to the line x= y (v-axis), and then it is converted using the same method as in Equations 1 and 2 but with the x and y directions switched, resulting on

$$v = U + \sqrt{2}F_2(-\frac{1}{\sqrt{2}}U + \frac{1}{\sqrt{2}}v) \quad (4)$$

V is stated as a function of u in equations (3) and (4). Equations (3) and (4) may be transformed into circuits with voltage-dependent voltage sources (3) and (4)[40]. The sine-like curve in "**figure 5"** depicts the difference between the two solutions, v1 and v2. **"figure 6"** is a circuit implementation of Equations 3 and 4 for mirrored SRAM flip-flop inverter curves [40]. The lengths of the diagonals of the squares inserted between the direct and mirrored SRAM flip-flop inverter curves are represented by the direct and values of the extremities of this curve (D), where dD/du = 0. The worst-case of an SRAM cell is obtained by multiplying the smaller of the two by ½.

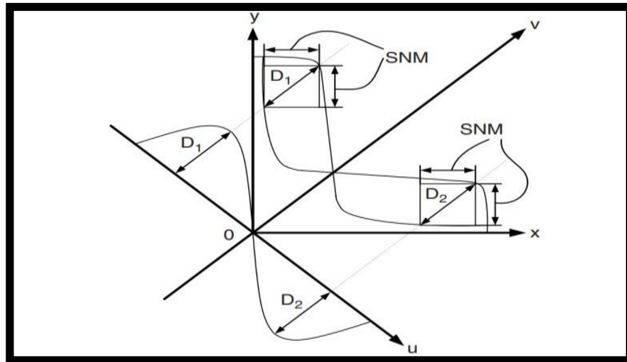

Figure 5: SNM estimation based on "maximum squares" in a 45° rotated coordinate system. The voltage transfer characteristics (VTCs) of both inverters comprising an SRAM cell are ideally symmetrical

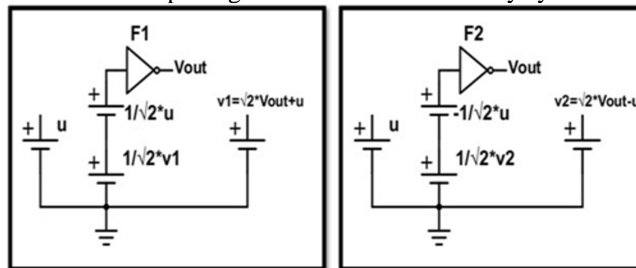

Figure 6.:Circuit implementation of Equations 3and 4 for finding the diagonal of the square embedded between the direct and mirrored SRAM flip-flop inverter curves.

IV. RESULT AND ANALYSIS

A. pCNFET Chirality Optimization at 0.9V Supply

With a supply voltage fixed at 0.9V, the chirality of the two pCNFETs is varied and the values are presented in table 1. Chirality of Pull-down and Access NCNFETs is (19,0) . CNFET Channel Length for all transistors =20nm. Gate-width of pull-up transistors (1tube) Wgate= 6.4nm. Gate- width of pull-down transistors (3tubes), Wgate = 25nm . Gate- width of access transistors (2tube), Wgate = 13nm. Taking Read SNM/(Write Time*Standby Power) as metric the parameters and their corresponding performance is obtained in table 2.

Table 1: PULL-UP PCNFET CHIRALITY OPTIMIZATION AT 0.9V SUPPLY FOR (n,0)

Chirality of PFET (n,0)	Read SMN (mV)	Write Time (ps)	Read SNM/Write time (mV/ps)
11	151.7	0.7104	213.54
13	156.1	0.7727	202.8
14	163.0	0.7988	204.06
16	173.4	0.8361	207.39
17	178.2	0.8528	208.96
19	188.1	0.8909	211.13
22	196.2	0.8655	226.7

TABLE 2: PULL-UP PCNFET CHIRALITY OPTIMIZATION AT 0.9V SUPPLY

Chirality of PFET	Stand by Power (pW)	Read SNM/ (Write time*Standby Power) (mV/ps-pW)
11	64.80	3.3
13	65	3.11
14	65.29	3.13
16	67.36	3.08
17	70	2.99
19	81.2	2.6
22	125.56	1.805

B. Access Transistor Channel Length (Lch) Optimization at 0.9V Supply

In all previous works of SRAM, tube numbers were used to determine this strength ratio. The strength of a short-channel nCNFET can be changed in another way, by simply changing its gate channel length. Chirality of Pull-down and Access NCNFETs is (19,0). Pull-up CNFET chirality (14,0). Channel Length for pull-up and pull-down transistors =20nm. No of nanotubes in pull-up pCNFET =1. No of nanotubes in pull-down nCNFET=3. No of nanotubes in access nCNFET =2. For the devices where power is an important concern, another performance metric Standby Power must be considered. Now, taking “Read SNM/(Write Time*Standby Power)” as the final figure of table 4 is obtained. Now, using values from table 3, both Read SNM and Write Time is plotted in the same graph in “**figure 7**” against channel length. A monotonic reduction of both the performance metrices

is observed as the channel length is increased from 10 nm to 15 nm.

TABLE 3:ACCESS NCNFET CHANNEL LENGTH OPTIMIZATION AT 0.9V SUPPLY

Channel length of access transistor (nm)	Read SNM (mV)	Write Time (ps)	Read SNM/Write time (mV/ps)
10	250.7	2.018	124.23
11	228.4	1.259	181.41
12	209.6	0.9981	210.00
13	196.2	0.8753	224.15
14	185.7	0.8113	228.89
15	177.7	0.7468	237.95
16	171.6	0.7215	238.13
17	167.3	0.7206	232.17
18	164.6	0.7417	221.92
19	163.2	0.7781	209.74
20	163.0	0.7988	204.06

TABLE 4:ACCESS NCNFET CHANNEL LENGTH OPTIMIZATION AT 0.9V SUPPLY AND CONSIDERING STANDBY POWER

Channel length of access transistor (nm)	Stand by Power (pW)	Read SNM/ (Write time*Standby Power) (mV/ps-pW)
10	32.73	3.79
11	33.26	5.45
12	34.36	6.11
13	36.11	6.21
14	38.64	5.92
15	41.94	5.67
16	45.93	5.18
17	50.44	4.60
18	55.29	4.01
19	60.30	3.48
20	65.29	3.12

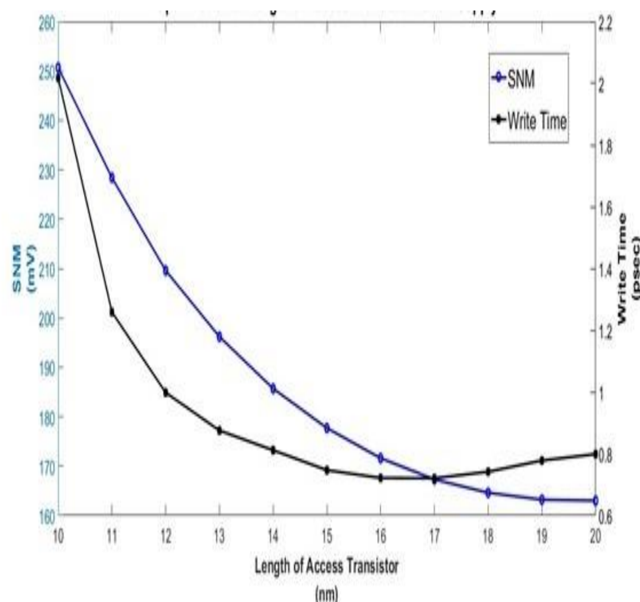

Figure 7.:Variation of Read SNM and Write as the channel length is varied.

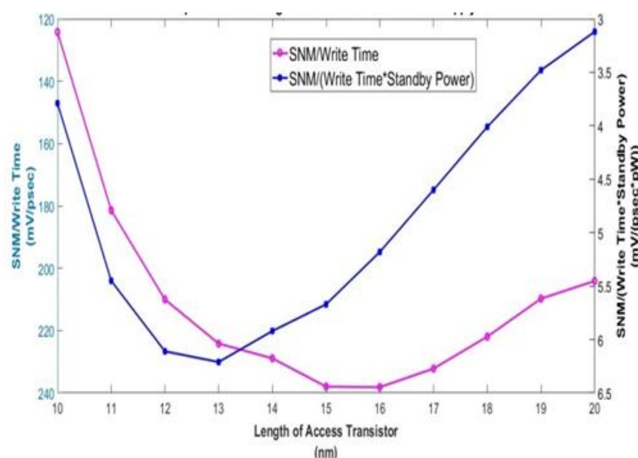

Figure 8: Graphical optimization of the channel length of the access transistors.

C. pCNFET Chirality Optimization at 0.7V Supply:

One way to reduce the power consumption of the device is to scale down the supply voltage. Since, these effects are quite severe in CMOS SRAM, it is important to know how the parameter optimized as the supply voltage is lowered below 0.9V. The simulations are done the same way as was done in sections 1 and 2. First, the optimum chirality of the pull-up pCNFET is obtained in table 5 for 0.7V supply. All other design parameters were kept the same as in section 1 Metallic CNTs are excluded from consideration. Taking Read SNM/(Write Time*Standby Power) as metric the performance data of table 6 is obtained.

TABLE 5:ACCESS NCNFET CHANNEL LENGTH OPTIMIZATION AT 0.7V SUPPLY

Chirality of PFET	Read SNM (mV)	Write Time (ps)	Read SNM/Write time (mV/ps)
11	99.78	0.8744	114.11
13	121.30	0.9036	134.24
14	128.10	0.9177	139.60
16	137.90	0.9177	139.60
17	141.50	0.9681	146.16
19	148.10	1.038	142.68
22	154.10	1.185	130.04

TABLE 6: ACCESS NCNFET CHANNEL LENGTH OPTIMIZATION AT 0.7V SUPPLY AND CONSIDERING STANDBY POWER.

Chirality of PFET	Standby Power (pW)	Read SNM/(Write time*Standby Power) (mV/ps-pW)
11	53.20	2.14
13	53.34	2.51
14	53.58	2.60
16	55.20	2.63
17	57.21	2.55
19	66.00	2.16
22	100.50	1.29

D. Access Transistor Channel Length(Lch) optimization at 0.7V Supply

The pull-down pCNFET chirality is taken as (16,0) as obtained in the previous section and the supply is lowered at 0.7V. Design Considerations: Chirality of Pull-down and Access NCNFETs is (19,0). Pull-up CNFET chirality (16,0). Channel Length for pull- up and pull-down transistors=20nm. No of nanotubes in pull-up pCNFET=1. No of nanotubes in pull-down nCNFET=3. No of nanotubes in access nCNFET=2. Now, we vary the channel length of the access transistors for a supply of 0.7V to obtain the corresponding performance data of table 7. Now, taking "Read SNM/(Write Time*Standby Power)" as the final figure of merit, it is obtained from table 8 that a channel length of 19nm is the best for power efficient operation at 0.7V supply. Now, using values from table 7, both Read SNM and Write Time is plotted in the same graph in **" figure 9"** against channel length, the variable.

TABLE 7: ACCESS NCNFET CHANNEL LENGTH OPTIMIZATION AT 0.7V SUPPLY AND CONSIDERING ACESS TRANSISTOR

Channel length of access transistor (nm)	**Read SNM (mV)**	**Write Time (ps)**	**Read SNM/Write time (mV/ps)**
10	257.4	Failed	-
11	235.3	Failed	-
12	213.8	5.767	37.07
13	196.2	2.516	77.98
14	181.8	1.722	105.23
15	170.0	1.402	121.25
16	160.3	1.206	132.92
17	152.7	1.075	142.05
18	146.6	1.005	145.87
19	141.7	0.9684	146.32
20	137.9	0.9483	145.42

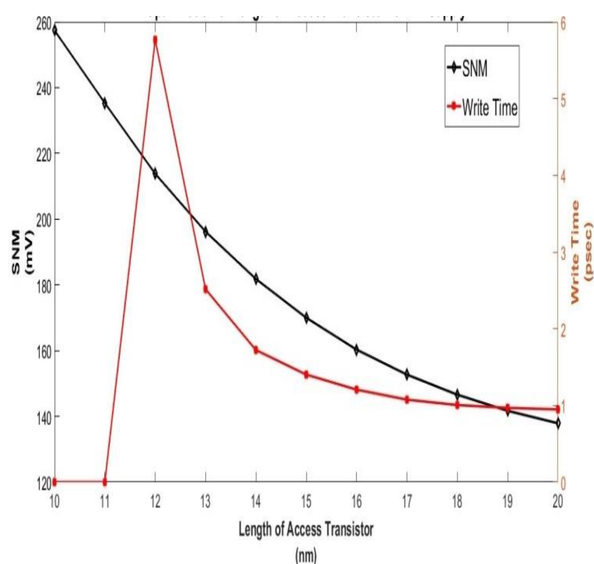

Figure 9: Variation of Read SNM and Write as the channel length is varied at 0.7 V supply

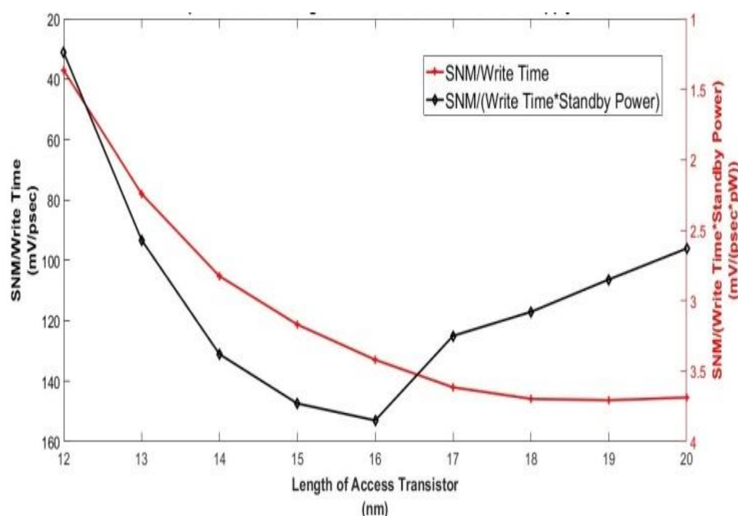

Figure 10 : Graphical optimization of the channel length of the access transistors at 0.7V supply

TABLE 8: ACCESS NCNFET CHANNEL LENGTH OPTIMIZATION

Channel length of access transistor	Standby Power (pW)	Read SNM/ (Write time*Standby Power) (mV/ps-pW)
10	29.91	-
11	30.32	-
12	31.17	1.24
13	32.52	2.57
14	34.49	3.38
15	37.05	3.73
16	40.15	3.85
17	43.66	3.25
18	47.43	3.08
19	51.32	2.85
20	55.20	2.63

E.Low-Voltage Performance Comparison among CNFET, FinFET and CMOS

The low voltage performance of the three processes is obtained by varying the supply from as low as 0.5V to 1.5V. The results for the Read SNM are given in table 9 below: Now, the bar-plot of "**figure 10**" is presented to better illustrate the data presented in table 9.

TABLE 9: ACCESS NCNFET CHANNEL LENGTH OPTIMIZATION AT 0.7V SUPPLY

Supply Voltage	CNFET Read SNM (mV)	CMOSRead SNM (mV	FinFETRead SNM (mV)
0.5V	99.58	207.6	207.2
0.6V	120.1	107.6	107.2
0.7V	137.6	7.811*	7.361
0.8V	155.2	89.55*	91.18

0.9V	173.4	169.7	184.8
1.0V	192.9	216.1	271.7
1.1V	205.8	241.0	352.3
1.2V	204.2	256.2	426.7
1.3V	223.6	266.8	493.3
1.4V	255.1	276.7	551.0
1.5V	292.6	291.9	601.5

Again, critical write time is simulated for 6T SRAM made from the three processes and the table 10 is obtained. Now, the plot of "**figure 11**" is presented to better illustrate the data presented in table 10.

TABLE 10: COMPARISON OF CRITICAL WRITE TIME AMONG CNFET, CMOS, FINFET PROCESSES

Supply Voltage	CNFET Write Time (ps)	CMOS Write Time (ps)	FinFETWrite Time (ps)
0.5V	2.179	3.127	52.49
0.6V	1.316	2.028	51.42
0.7V	0.9483	1.635	49.82
0.8V	0.8689	1.446	47.15
0.9V	0.8361	1.345	43.86
1.0V	0.7817	1.280	40.37
1.1V	0.6557	1.234	36.87
1.2V	0.6441	1.202	33.60
1.3V	0.6214	1.174	30.64
1.4V	0.6278	1.152	27.95
1.5V	0.6679	1.131	25.56

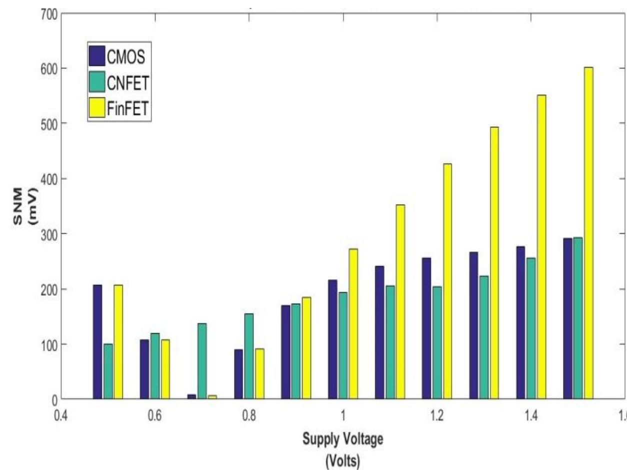

Figure 11 : SNM comparison among CNFET, CMOS and FinFET processes.

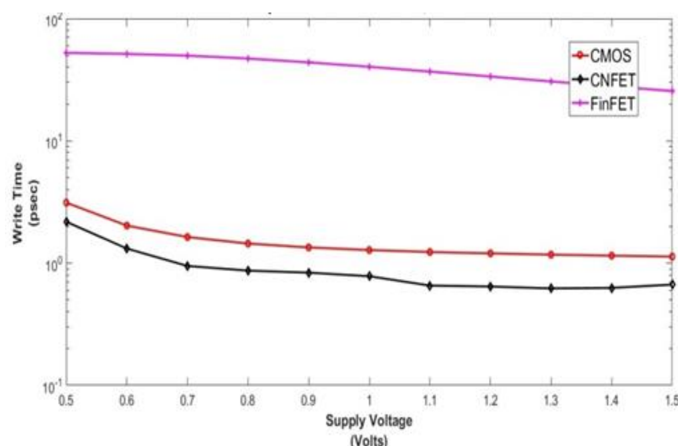

Figure 12 : Comparison of Write-Time among CNFET, CMOS and FinFET processes

A simulation is also done about standby power of table 11 for the 6T SRAMs made from CNFET, CMOS and FinFET. As observed, standby power clearly decreases as supply voltage is scaled, but it doesn't decrease at the same rate for all three processes. Now, the plot of "**figure 13**" is presented to better illustrate the data presented in table 11.

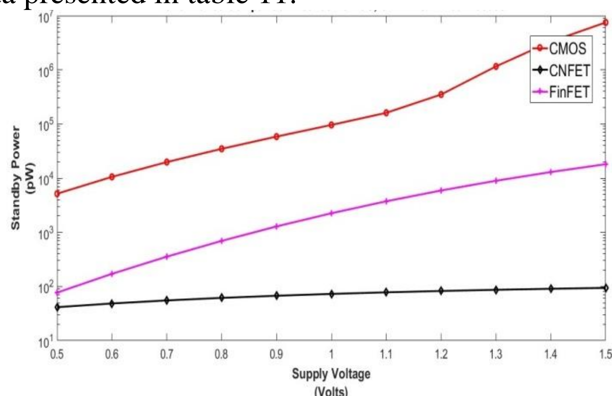

Figure 13: Comparison of Standby Power among CNFET, CMOS and FinFET processes

TABLE 11: COMPARISON OF STANDBY POWER AMONG CNTFET, CMOS, FINFET PROCESSES

Supply Voltage	CNFET Standby Power (pW)	CMOS Standby Power (pW)	FinFET Standby Power (pW)
0.5	41.41	5150	76.91
0.6	48.50	10560	170.9
0.7	55.20	19790	354.9
0.8	61.49	34800	693.3
0.9	67.36	58490	1283
1.0	72.81	95990	2247
1.1	77.83	160700	3738
1.2	82.49	350500	5918
1.3	86.74	1157000	8947

1.4	90.60	3321000	12970
1.5	94.04	748000	18100

To decide which one the superior of the three, the performance metric that can be used is the ratio of the read SNM and product of write time and leakage power. With the data obtained in Table 9 to 11, a bar-graph is plotted in "**figure 14**" of the performance metric against different supply. It can be clearly seen that, CNFET is a much better choice in all the voltages of interest.

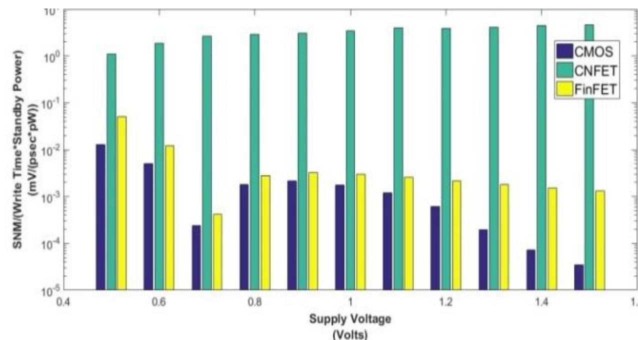

Figure 14 :Overall performance comparison among CNFET, CMOS and FinFET processes voltages.

F . Performance Comparison among CNFET, Fin- FET and CMOS with Temperature Variation

SNM data is obtained for the three processes by varying temperature from -30°C to 60°C . The plot is given in "**figure 15**". In "**figure 15**" it is observed that the SRAM using CNFET process can have a stable SNM performance over a wide range of temperatures while the performance of the other two either degrade or vary significantly with the increase of temperature. In fact, SNM of CNTFET process decreases from 0.195mV to 0.183mV as the temperature increases from -30°C to 60°C , a degradation of only 6.15% in a 90°C. While, the SNM for the FinFET process, though has a promising SNM value of .205mV for -30°C, it quickly degrades to .180mV for 60°C temperature, a degradation of about 12.2%. SNM for CMOS, although doesn't vary much (from .180mV to .165mV about 8.33%) it is poorer than the other two throughout the temperature range of interest. So, clearly, to get a stable and satisfactory performance from the memory circuit in a wide range of temperatures, CNFET should be the right choice.

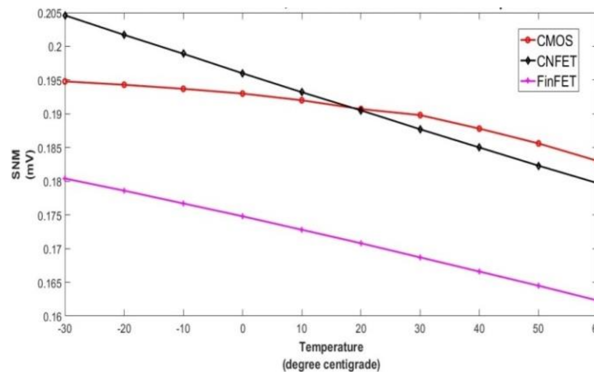

Figure 15: Temperature variation of SNM of three processes.

V. Conclusion

A. Summary of this research

In this research, CNTFET models and their device physics, especially the Stanford CNFET Model is studied. Using this model in HSPICE, different performance metrices of a CNTFET based SRAM CELL are obtained. The three SRAM performance matrices are Static Noise Margin, Critical Write Time and Leakage Power. First, a methodology of calculating the SNM using HSPICE was studied, then using that method SNM datas were obtained for CNTFET SRAM CELL. A comparison among these three matrices; CNTFET, CMOS and FinFET was obtained. After that, a superior performance CNTFET was designed by optimizing its different parameters such as chirality, channel length etc. The other two process models were implemented using PTM (Predictive Technology Model) such as for the CMOS, the model was PTM 22nm Metal Gate / High-K and for the FinFET it was PTM 20nm LSTP. It is observed that,

1) CNTFET has moderate SNM overall and in the range of 0.7V- 0.8V much better SNM than others.
2) FinFET has superior SNM at higher voltages but at the cost of 30 times more Write-time than CNT.
3) CMOS has very large standby power making it unsuitable for SRAM design.
4) The overall performance matric is much better for CNTFET than the other two.

5.2. Recommendations for Future Work

The CNTFET model that is used in this work has a planar gate structure. There are a lot of prospective geometries of CNTFETs such as cylindrical CNTFETs, back-gated and top-gated CNTFETS which might be studied and simulated to observe their performance as a memory transistor. Then a comparison among them can be done as to which geometry is better to be used in the SRAM CELL design. Again, this thesis only obtained the parameters that yielded the best design, it neither predicts nor propose any method to calculate the best parameters. An analytical relation should be formulated as to predict how the three performance matrices SNM, writability and power are affected by CNTFET parameter change. The proposed optimum parameter CNTFET based SRAM Cell shows great performance improvements but the speed of the circuit is still slightly lower than its CMOS. Compensation circuit can be used to improve the performance further. Again, using HSPICE for simulation has not converged for lower voltage levels. High-speed processors enable the use of more precise models, such as NEGF and Monte-Carlo simulations, to provide simulation results that are more accurate.

COMPETING INTERESTS

The authors have no compting interest to declare.

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